Features

- Frequency band: 2402~2480MHz
- Supports 3-wire or 4-wire SPI interface
- Wide input voltage range of 1.9V~3.6V
- Programmable data rate: 125/250/500Kbps
- Programmable TX output power up to 5dBm (Max. +6dBm)
- Low current consumption
  - 0.5μA deep sleep mode current with data retention
  - TX current: 25mA@5dBm
  - RX current: 17mA@250Kbps
- Dual sleep modes
  - Middle sleep mode to support fast XO start-up
  - Regular light sleep mode
- RX sensitivity
  - -97dBm at 250Kbps on-air data rate
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports 16MHz crystal (±20ppm)
- Packet handling
  - Data whitening
  - Auto-ACK/Resend
  - CRC optional protocol
  - Support Burst packets
  - Support Automatic ACK transaction
  - 6 data-pipes for 1:6 star network
- FCC/ETSI Compiant
- Package type: 16-pin QFN (3mm×3mm)

General Description

The BC5602 is a high performance and low cost fully-integrated CMOS RF GFSK transceiver for wireless applications in the 2.4GHz frequency band. It incorporates a highly integrated 2.4GHz transceiver and a baseband modem with programmable data rates of 125Kbps, 250Kbps and 500Kbps. Data handling features include 3 levels of 32-byte TX/RX FIFO and packet handling such as whitening and CRC checking.

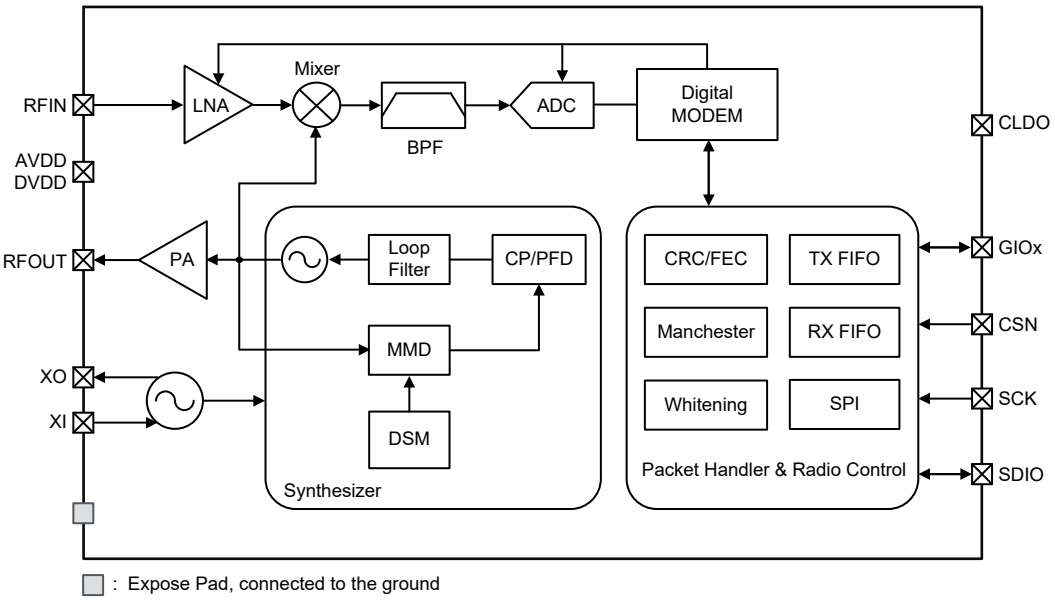
The BC5602 supports a Middle Sleep mode for fast XO start-up with 30μA bleeding current. At 2.4GHz, the BC5602 can achieve -97dBm sensitivity at 250Kbps and deliver +5dBm TX output power at 25mA current. A fully integrated Fractional-N synthesizer can support a wide frequency range with a fine resolution.

External host MCU can access the BC5602 through a 3-wire or 4-wire SPI interface. The device supports short strobe commands to reduce the loading of the host MCU while maintaining wireless communication link.

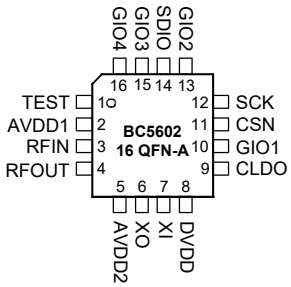
Additional link layer features like RSSI for channel assessment, auto-acknowledgement, auto-resend and 6 pipes star network topology, facilitate microcontroller based ISM bands wireless link applications.

The BC5602 is also fully compatible with the BC516x series transmitter to pair with each other for the receiver role, which not only supports packet format but also supports all kinds of data rates for remote control related applications.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	Type	Description
1	TEST	—	Analog test pin
2	AVDD1	PWR	Analog power supply
3	RFIN	AI	RF LNA input
4	RFOUT	AO	RF power amplifier output
5	AVDD2	PWR	Analog power supply
6	XO	AO	Crystal oscillator output
7	XI	AI	Crystal oscillator input
8	DVDD	PWR	Digital power supply
9	CLDO	PWR	LDO output, connected to a bypass capacitor
10	GIO1	DI/O	Multi-function I/O 1
11	CSN	DI	SPI chip select input, low active
12	SCK	DI	SPI clock input

Pin No.	Pin Name	Type	Description
13	GIO2	DI/O	Multi-function I/O 2
14	SDIO	DI/O	SPI data input/output
15	GIO3	DI/O	Multi-function I/O 3
16	GIO4	DI/O	Multi-function I/O 4
EP	GND	PWR	Ground

Legend: DI: Digital Input; DI/O: Digital Input/Output; AI: Analog Input; AO: Analog Output; PWR: Power.

The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to 3.6V

Voltage on I/O Pins ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -50°C to 125°C

Operating Temperature ..... -40°C to 85°C

ESD HBM ..... ±2KV

* The device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those has listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, GFSK modulation with matching circuit and low/high pass filter, RF output is powered by V_{DD} (3.3V), unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	–	85	°C
V_{DD}	Supply Voltage	—	1.9	3.3	3.6	V
Digital I/Os						
V_{IH}	High Level Input Voltage	—	0.7×V_{DD}	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	0.3×V_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH}=-5mA	0.8×V_{DD}	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL}=5mA	0	—	0.2×V_{DD}	V
Current Consumption						
I_{Sleep}	Deep Sleep Mode Current	—	—	0.5	—	μA
I_{IL1}	Middle Sleep Mode Current	X'tal on under bleeding current	—	30	—	μA
I_{IL2}	Light Sleep Mode Current	X'tal on	—	400	—	μA
$I_{Standby}$	Standby Mode Current	X'tal on, Synthesizer on	—	7	—	mA
I_{RX} or I_{TX}	RX or TX Mode Current	RX mode @ 250Kbps	—	17	—	mA
		RX mode @ 500Kbps	—	17	—	mA
		TX mode @ 0dBm P_{OUT}	—	17	—	mA
		TX mode @ 5dBm P_{OUT}	—	25	—	mA

A.C. Characteristics

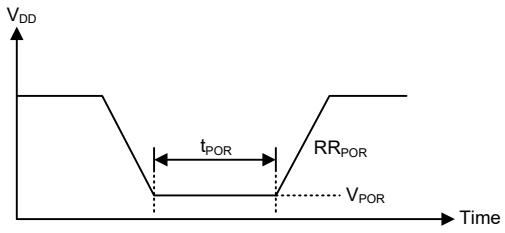
Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, GFSK modulation with matching circuit and low/high pass filter, RF output is powered by V_{DD} (3.3V), unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RF Characteristics						
f_{RF}	RF Frequency Band	—	2402	—	2480	MHz
DR	Data Rate	GFSK modulation	125	—	500	Kbps
Transmitter						
$t_{ST,TX}$	TX Settling Time	Light Sleep mode to TX mode	—	TBD	—	μs
P_{OUT}	TX Output Power	2400~2483MHz	-10	5	6	dBm
S.E.$_{TX}$	TX Spurious Emission	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz 87.5MHz < f < 118MHz 174MHz < f < 230MHz 470MHz < f < 862MHz	—	—	-54	
		2nd, 3rd Harmonic	—	—	-30	
		1.8GHz~1.9GHz	—	—	-47	
		5.15GHz~5.3GHz	—	—	-47	
Receiver						
$t_{ST,RX}$	RX Settling Time	Light Sleep mode to RX mode	—	TBD	—	μs
P_{Sens}	RX Sensitivity @ BER=0.1%	125Kbps (f_{DEV}=160kHz)	—	-98	—	dBm
		250Kbps (f_{DEV}=160kHz)	—	-97	—	
		500Kbps (f_{DEV}=250kHz)	—	-92	—	
$P_{IN,max}$	Maximum Input Power	@ BER<0.1%	—	—	10	dBm
IR	Image Rejection	—	—	30	—	dB
S.E.$_{RX}$	RX Spurious	25MHz~1GHz	—	—	-57	dBm
		Above 1GHz	—	—	-47	
	RSSI Range	AGC on	-110	—	-10	dBm
LO Characteristics						
f_{LO}	RF Frequency Coverage Range	—	2380	—	2520	MHz
PN_{LO}	Phase Noise	@ 100kHz offset	—	-85	—	dBc/Hz
		@ 1MHz offset	—	-95	—	
	PLL ready from Sleep Mode (49US XO)	Deep Sleep mode to RX mode ready	—	TBD	—	μs
		Middle Sleep mode to RX mode ready	—	TBD	—	μs
Crystal Oscillator						
f_{XTAL}	X'tal Frequency	—	—	16	—	MHz
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C_{LOAD}	X'tal Capacitor Load	—	12	—	16	pF
TOL	X'tal Tolerance	—	-20	—	+20	ppm
t_{SU}	X'tal Startup Time	49US with a 12pF C_{LOAD}	—	—	1	ms
		3225 SMD with a 12pF C_{LOAD}	—	3	—	ms

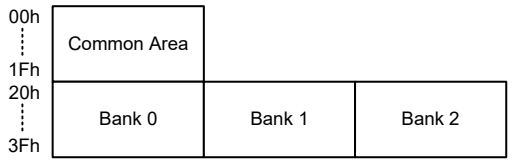
Power on Reset Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms



Memory Mapping

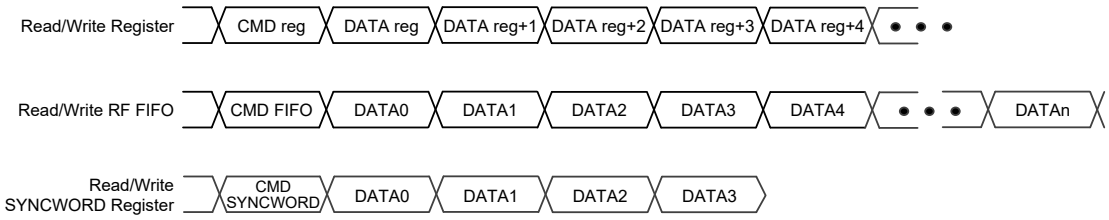


Common Area: It is independent of Bank Pointer setting and has a total space of 32 bytes.

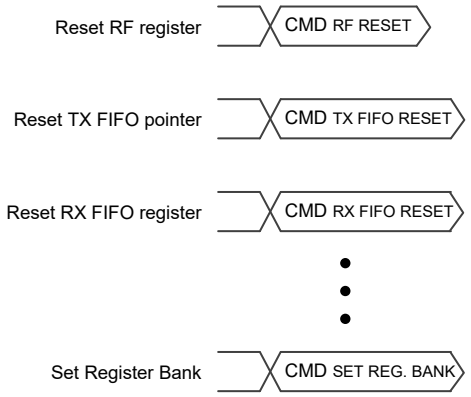
Bank 0~2: Selected by Bank Pointer Register. The total space of the area is up to 128 bytes (4×32 bytes).

The Bank Pointer can be set directly by the Set Register Bank command which is also defined in Common Area and can be read or written by the Control Register command too.

Control Register Access



Strobe Command Followed by n-byte Data (CmdD)



Strobe Command Only (CmdO)

Special Function Register

Common Area Control Register

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG1	—	AGC_EN	—	DIR_EN	—	—	BANK[1:0]	
01h	RC1	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RSTLL
02h	RSV1	—	—	Reserved		—	—	—	Reserved
03h	MASK	—	MASK_RX	MASK_TX	MASK_MAX_RT	—	—	—	PRM_RX
04h	IRQ1	—	RX_DR	TX_DS	MAX_RT	RX_P_NO[2:0]			TX_FULL
05h	STATUS	—	—	TX_FULL	TX_EMPTY	—	—	RX_FULL	RX_EMPTY
06h	IO1	PADDS[1:0]		GIO2S[2:0]		GIO1S[2:0]			
07h	IO2	GIO4S[3:0]				GIO3S[3:0]			
08h	IO3	SDO_TEN	SPIPU	—	GIOPU[4:1]				—
09h	PKT1	—	—	CRC_EN	CRC8_EN	—	—	—	—
0Ah	PKT2	WHT_EN	WHTSD[6:0]						
0Bh	PKT3	WHT_PCF_EN	—						
0Ch	PKT4	RXDLEN[7:0]							
0Dh	RSV2	—	Reserved			—	Reserved		
0Fh	RSV3	—	—	—	Reserved	Reserved		Reserved	—
10h	RFCH	—	RF_CH[6:0]						
11h	DM1	AW[1:0]		—	—	—	MDIV_SEL	SDR[1:0]	
13h	RT1	ARD[3:0]				ARC[3:0]			
14h	RT2	CNT_PLOS[3:0]				CNT_ARC[3:0]			
15h	CE	—	—	—	—	—	—	—	CE
16h	RSV4	Reserved							
17h	RSV5	Reserved							
18h	RSV6	Reserved							

Note: Addresses 0Eh, 12h and 19h~1Fh which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The recommended values for the Common Bank 02h, 0Dh, 0Fh and 16h~18h registers are listed below:

Addr	Name	Setting
02h	RSV1	00h
0Dh	RSV2	26h
0Fh	RSV3	14h
16h	RSV4	66h
17h	RSV5	AAh
18h	RSV6	45h

- **CFG1: Configuration Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	AGC_EN	—	DIR_EN	—	—	BANK[1:0]	
R/W	—	R/W	—	R/W	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

Bit 7 Reserved, must be kept unchanged after power on

Bit 6 **AGC_EN**: AGC enable
0: Disable
1: Enable

Bit 5 Reserved, must be kept unchanged after power on

Bit 4 **DIR_EN**: Direct mode enable
0: TX/RX data from packet handling hardware
1: TX/RX data from/to external MCU directly

Bit 3~2 Reserved, must be kept unchanged after power on

Bit 1~0 **BANK[1:0]**: Control register bank selection
00: Bank 0
01: Bank 1
10: Bank 2
11: Reserved
This selection can be set by both the Set Register Bank command and Control Register command.

- **RC1: Reset/Clock Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RSTLL
R/W	R/W	R	R	R/W	R/W		R/W	R/W
Reset	1	0	0	1	0	0	0	0

Bit 7 **PWRON**: 3.3V power on flag

This bit is only set to 1 by power on reset and not affected by software reset of strobe command. After being set high, this bit should be cleared by application program. The firmware can check this flag status and determine whether to execute auto calibration in the Light Sleep mode.

Bit 6 **FSYCK_RDY**: FSYCK clock ready flag (ready only)

0: Not ready

1: Ready

This bit is used to indicate that whether the FSYCK clock is ready for operation. This bit will be automatically cleared when FSYCK_EN=0, when power on reset occurs or when a Deep Sleep command or a Middle Sleep command is received.

Bit 5 **XCLK_RDY**: XCLK clock ready flag (ready only)

0: Not ready

1: Ready

This bit is used to indicate whether the XCLK debounce counter is full and XCLK is ready for operation. Note that when exiting the Deep Sleep state, this flag may need a certain period before being set high. This bit will be automatically cleared to zero when XCLK_EN=0, when RSTLL=1, when power on reset occurs or when a software reset command, a Deep Sleep command or a Middle Sleep command is received.

Bit 4 **XCLK_EN**: XCLK clock enable

0: Disable

1: Enable

Setting this bit high will enable the XCLK path to the baseband block while clearing this bit to zero can save power if required. The XCLK clock should be enabled when writing data to the FIFO.

Bit 3~2 **FSYCK_DIV[1:0]**: FSYCK clock selection

00: 1/1 XCLK

01: 1/2 XCLK

10: 1/4 XCLK

11: 1/8 XCLK

Bit 1 **FSYCK_EN**: FSYCK clock enable

0: Disable

1: Enable

Bit 0 **RSTLL**: Low voltage (1.2V) logic reset control

0: Release reset

1: Reset

- **MASK: Mask Control Register**

Bit	7	6	5	4	3	2	1	0
Name	—	MASK_RX	MASK_TX	MASK_MAX_RT	—	—	—	PRM_RX
R/W	—	R/W	R/W	R/W	—	—	—	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 Reserved, must be kept unchanged after power on

Bit 6 **MASK_RX**: Mask RX_DR interrupt
0: Enable RX_DR interrupt
1: Mask RX_DR interrupt

Bit 5 **MASK_TX**: Mask TX_DS interrupt
0: Enable TX_DS interrupt
1: Mask TX_DS interrupt

Bit 4 **MASK_MAX_RT**: Mask MAX_RT interrupt
0: Enable MAX_RT interrupt
1: Mask MAX_RT interrupt

Bit 3~1 Reserved, must be kept unchanged after power on

Bit 0 **PRM_RX**: PTX or PRX device setting
0: PTX device
1: PRX device

- **IRQ1: Interrupt Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	RX_DR	TX_DS	MAX_RT	RX_P_NO[2:0]			TX_FULL
R/W	—	R/W	R/W	R/W	R			R
Reset	0	0	0	0	1	1	1	0

Bit 7 Reserved, must be kept unchanged after power on

Bit 6 **RX_DR**: RX data received into RX FIFO interrupt
0: RX data is not received into RX FIFO
1: RX data is received into RX FIFO
This flag will be set high by hardware when the RX data is received into RX FIFO and should be cleared by writing "1" to it.

Bit 5 **TX_DS**: TX data sent from TX FIFO interrupt
0: TX data is not sent from TX FIFO
1: TX data is sent from TX FIFO
This flag will be set high by hardware when the TX data is sent from TX FIFO and should be cleared by writing "1" to it.

Bit 4 **MAX_RT**: Preset number of TX retransmissions interrupt
0: The preset number of TX retransmissions is not finished
1: The preset number of TX retransmissions is finished
This flag will be set high by hardware when the preset number of TX retransmissions is finished and should be cleared by writing "1" to it.

Bit 3~1 **RX_P_NO[2:0]**: Data pipe number for the payload available for reading from RX FIFO

Bit 0 **TX_FULL**: TX FIFO full Flag
0: TX FIFO is not full
1: TX FIFO is full

- **STATUS: FIFO Status Control Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TX_FULL	TX_EMPTY	—	—	RX_FULL	RX_EMPTY
R/W	—	—	R	R	—	—	R	R
Reset	0	0	0	1	0	0	0	1

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5 **TX_FULL**: TX FIFO full Flag
0: TX FIFO is not full
1: TX FIFO is full

Bit 4 **TX_EMPTY**: TX FIFO empty Flag
0: TX FIFO is not empty
1: TX FIFO is empty

Bit 3~2 Reserved, must be kept unchanged after power on

Bit 1 **RX_FULL**: RX FIFO full Flag
0: RX FIFO is not full
1: RX FIFO is full

Bit 0 **RX_EMPTY**: RX FIFO empty Flag
0: RX FIFO is not empty
1: RX FIFO is empty

- **IO1: I/O Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PADDS[1:0]		GIO2S[2:0]			GIO1S[2:0]		
R/W	R/W		R/W			R/W		
Reset	0	1	0	0	0	0	0	0

Bit 7~6 **PADDS[1:0]**: PAD current control
00: 0.5mA
01: 1mA
10: 5mA
11: 10mA

Bit 5~3 **GIO2S[2:0]**: GIO2 pin function selection (only reset by POR)
000: No function, input
001: SDO, 4-wire SPI data, output
101: IRQ, interrupt request, output
Others: No function, input

Bit 2~0 **GIO1S[2:0]**: GIO1 pin function selection (only reset by POR)
000: No function, input
001: SDO, 4-wire SPI data, output
101: IRQ, interrupt request, output
Others: No function, input

- **IO2: I/O Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	GIO4S[3:0]				GIO3S[3:0]			
R/W	R/W				R/W			
Reset	0	0	0	0	0	0	0	0

Bit 7~4 **GIO4S[3:0]**: GIO4 pin function selection (only reset by POR)

0000: No function, input

0001: SDO, 4-wire SPI data, output

0101: IRQ, interrupt request, output

1010: FSYCK, i.e. XCLK 1/1, 1/2, 1/4, 1/8 output

1100: EPA_EN, external PA enable, output

1101: ELAN_EN, external LNA enable, output

Others: No function, input

Bit 3~0 **GIO3S[3:0]**: GIO3 pin function selection (only reset by POR)

0000: No function, input

0001: SDO, 4-wire SPI data, output

0101: IRQ, interrupt request, output

1010: FSYCK, i.e. XCLK 1/1, 1/2, 1/4, 1/8 output

1100: EPA_EN, external PA enable, output

1101: ELAN_EN, external LNA enable, output

Others: No function, input

- **IO3: I/O Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	SDO_TEN	SPIPU	—	GIOPU[4:1]				—
R/W	R/W	R/W	—	R/W				—
Reset	0	1	1	1	1	1	1	1

Bit 7 **SDO_TEN**: SDO tri-state enable (only reset by POR)

0: Disable

1: Enable

Bit 6 **SPIPU**: 3-wire SPI pull-up enable (only reset by POR)

0: Disable

1: Enable

When this bit is set high, it only controls the pull-up function for the CSN, SCK and SDIO pins. Note that the pull-up function of the SDO pin for the 4-wire SPI is configured using the GIOPU[4:1] bits.

Bit 5 Reserved, must be kept unchanged after power on

Bit 4~1 **GIOPU[4:1]**: GIO pin function pull-up enable control (only reset by POR)

These bits control the pull-high function of the GIO4~GIO1 pins respectively.

Bit 0 Reserved, must be kept unchanged after power on

- **PKT1: Packet Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	CRC_EN	CRC8_EN	—	—	—	—
R/W	—	—	R/W	R/W	—	—	—	—
Reset	0	0	1	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5 **CRC_EN**: CRC field enable
0: Disable
1: Enable

Bit 4 **CRC8_EN**: CRC format selection
0: CRC16 = $X^{16}+X^{12}+X^5+1$
1: CRC8 = X^8+X^2+X+1

Bit 3~0 Reserved, must be kept unchanged after power on

- **PKT2: Packet Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	WHT_EN	WHTSD[6:0]						
R/W	R/W	R/W						
Reset	0	0	1	1	0	1	1	0

Bit 7 **WHT_EN**: Data whitening enable
0: Disable
1: Enable

Bit 6~0 **WHTSD[6:0]**: Data whitening seed

- **PKT3: Packet Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	WHT_PCF_EN	—	—	—	—	—	—	—
R/W	R/W	—	—	—	—	—	—	—
Reset	0	0	0	0	0	0	0	0

Bit 7 **WHT_PCF_EN**: Data whitening range selection
0: Packet Control Field (PCF) is not included
1: Packet Control Field (PCF) is included

Bit 6~0 Reserved, must be kept unchanged after power on

- **PKT4: Packet Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	RXDLEN[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RXDLEN[7:0]**: RX FIFO data payload length

- **RFCH: RF Channel Setting Register**

Bit	7	6	5	4	3	2	1	0
Name	—	RF_CH[6:0]						
R/W	—	R/W						
Reset	0	0	0	0	0	0	1	0

Bit 7 Reserved, must be kept unchanged after power on

Bit 6~0 **RF_CH[6:0]**: RF channel setting

Real RF TX frequency = (2400+RF_CH[6:0])MHz

- **DM1: De-modulator Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	AW[1:0]		—	—	—	MDIV_SEL	SDR[1:0]	
R/W	R/W		—	—	—	R/W	R/W	
Reset	1	1	0	0	0	0	0	0

Bit 7~6 **AW[1:0]**: TRX Sync words (Sync Address or Sync ID) length control

00: Illegal

01: 3 bytes

10: 4 bytes

11: 5 bytes

Bit 5~3 Reserved, must be kept unchanged after power on

Bit 2~0 **MDIV_SEL, SDR[1:0]**: TRX data rate selection

000: 500Kbps

001: 250Kbps

010: 125Kbps

Others: Reserved

- **RT1: PTX Retransmission Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	ARD[3:0]				ARC[3:0]			
R/W	R/W				R/W			
Reset	0	0	0	0	0	0	1	1

Bit 7~4 **ARD[3:0]**: Auto retransmission delay control

0000: wait 250μs	0001: wait 500μs	0010: wait 750μs	0011: wait 1000μs
0100: wait 1250μs	0101: wait 1500μs	0110: wait 1750μs	0111: wait 2000μs
1000: wait 2250μs	1001: wait 2500μs	1010: wait 2750μs	1011: wait 3000μs
1100: wait 3250μs	1101: wait 3500μs	1110: wait 3750μs	1111: wait 4000μs

Bit 3~0 **ARC[3:0]**: Auto retransmission count

0000: Disable retransmission function

0001: Up to 1 retransmission for TX payload

0010: Up to 2 retransmissions for TX payload

...

1111: Up to 15 retransmissions for TX payload

- **RT2: PTX Retransmission Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	CNT_PLOS[3:0]				CNT_ARC[3:0]			
R/W	R				R			
Reset	0	0	0	0	0	0	0	0

Bit 7~4 **CNT_PLOS[3:0]**: Lost packet counting in the same RF_CH
The counter is overlow protected by 15 and is cleared when setting RF_CH.

Bit 3~0 **CNT_ARC[3:0]**: Retransmitted packet counting

- **CE: Chip Enable Control Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	CE
R/W	—	—	—	—	—	—	—	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7~1 Reserved, must be kept unchanged after power on

Bit 0 **CE**: Chip enable control
0: Disable
1: Enable
If the device is set as a PTX device and the CE bit is set high, it will stay in the Light Sleep mode when the TX FIFO is empty. The PTX device will enter the TX mode automatically once the TX FIFO is not empty. After each packet transmission is finished, the PTX device will return to and stay in the Light Sleep mode if the TX FIFO is empty, or enter the TX mode automatically again if the TX FIFO is still not empty. If users want the PTX device to enter in the Light Sleep mode when the TX FIFO is not empty, the CE bit must be cleared to zero.
If the device is set as a PRX device, it will enter the RX mode when the CE bit is set high by using register or using Strobe RX command. After each packet transmission is finished (ACK or No-ACK), the PRX device will enter the RX mode automatically if the CE bit is still high. Users can use the Light Sleep command or clear this register to make CE=0. When the CE bit is cleare to 0, the state machine will stop the RX operation and make the device enter the Light Sleep mode.

Bank 0 Control Register

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
20h	OM	—	—	—	—	ACAL_EN	—	—	—
21h	CFO1	ACFO_EN	AMBLE2	—	—	—	—	—	—
26h	STA1	—	—	—	—	—	OMST[2:0]		
27h	RSSI1	—				RSSI_CTHD[3:0]			
28h	RSSI2	RSSI_NEGDB[7:0]							
29h	RSSI3	RSSI_SYNC_OK[7:0]							
2Ah	DPL1	—	—	DPL_P5	DPL_P4	DPL_P3	DPL_P2	DPL_P1	DPL_P0
2Bh	DPL2	INV_NOACK	—	—	—	—	EN_DPL	EN_ACK_PLD	EN_DYN_ACK
2Ch	RXPW0	—	—	RX_PW_P0[5:0]					
2Dh	RXPW1	—	—	RX_PW_P1[5:0]					
2Eh	RXPW2	—	—	RX_PW_P2[5:0]					
2Fh	RXPW3	—	—	RX_PW_P3[5:0]					
30h	RXPW4	—	—	RX_PW_P4[5:0]					
31h	RXPW5	—	—	RX_PW_P5[5:0]					
32h	ENAA	—	—	ENAAP5	ENAAP4	ENAAP3	ENAAP2	ENAAP1	ENAAP0
33h	P2B0	P2B0[7:0]							
34h	P3B0	P3B0[7:0]							

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
35h	P4B0	P4B0[7:0]							
36h	P5B0	P5B0[7:0]							
37h	PEN	—	—	P5ACTIVE	P4ACTIVE	P3ACTIVE	P2ACTIVE	P1ACTIVE	P0ACTIVE
38h	XO1	—	—	XO_IL	XO_TRIM[4:0]				

Note: Addresses 22h~25h and 39h~3Fh are not listed in this table and are reserved for future use, it is suggested not to change their initial values by any methods.

- **OM: Operation Mode Control Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	ACAL_EN	—	—	—
R/W	—	—	—	—	R/W	—	—	—
Reset	0	0	0	0	0	0	0	0

Bit 7~4 Reserved, must be kept unchanged after power on

Bit 3 **ACAL_EN**: Auto calibration enable

0: Disable

1: Enable

When this bit is set high, the VCO calibration will be enabled. When the VCO calibration is completed, this bit will be cleared to zero by hardware.

Bit 2~0 Reserved, must be kept unchanged after power on

- **CFO1: Carrier Frequency Offset Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	ACFO_EN	AMBLE2	—	—	—	—	—	—
R/W	R/W	R/W	—	—	—	—	—	—
Reset	0	0	0	0	1	1	1	1

Bit 7 **ACFO_EN**: Auto CFO calculations enable

0: Disable

1: Enable

Bit 6 **AMBLE2**: Preamble length selection

0: 1 byte

1: 2 bytes

Bit 5~0 Reserved, must be kept unchanged after power on

- **STA1: Status Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	OMST[2:0]		
R/W	—	—	—	—	—	R		
Reset	0	0	0	0	0	0	0	0

Bit 7~3 Reserved, must be kept unchanged after power on

Bit 2~0 **OMST[2:0]**: Operation mode state indication (read only)

000: Deep Sleep mode
001: Middle Sleep mode
010: Light Sleep mode
011: Standby mode
100: TX mode
101: RX mode
110: Calibration mode
111: Undefined

- **RSSI1: RSSI Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSSI_CTHD[3:0]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	1	0	1	0

Bit 7~4 Reserved, must be kept unchanged after power on

Bit 3~0 **RSSI_CTHD[3:0]**: RSSI threshold for carrier detection (unit: -dBm)
(RSSI_CTHD[3:0]×2+1)+74=RSSI threshold for carrier detection

- **RSSI2: RSSI Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	RSSI_NEGDB[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RSSI_NEGDB[7:0]**: RSSI value (unit: -dB)
It is a real time measurement value.

- **RSSI3: RSSI Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	RSSI_SYNC_OK[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RSSI_SYNC_OK[7:0]**: RSSI snapshot when Sync Word is mached

- **DPL1: Dynamic Payload Length Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	DPL_P5	DPL_P4	DPL_P3	DPL_P2	DPL_P1	DPL_P0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **DPL_P[5:0]**: Dynamic Payload Length Control for each pipe
DPL_Pn=0: Work in fixed payload length mode
DPL_Pn=1: Work in dynamic payload length mode when EN_DPL=1

- **DPL2: Dynamic Payload Length Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	INV_NOACK	—	—	—	—	EN_DPL	EN_ACK_PLD	EN_DYN_ACK
R/W	R/W	—	—	—	—	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 **INV_NOACK**: NO_ACK bit function control
0: NO_ACK=1 bit means No-Need-to-ACK
1: NO_ACK=1 bit means Need-to-ACK

Bit 6~3 Reserved, must be kept unchanged after power on

Bit 2 **EN_DPL**: Dynamic payload length enable
0: Disable
1: Enable

Bit 1 **EN_ACK_PLD**: PRX acknowledge with payload function enable
0: Disable
1: Enable

Bit 0 **EN_DYN_ACK**: PTX "write TX FIFO with No-Auto-ACK" command enable
0: Disable
1: Enable

- **RXPW0: RX Payload Length Control Register 0**

Bit	7	6	5	4	3	2	1	0
Name	—	—	RX_PW_P0[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **RX_PW_P0[5:0]**: Pipe 0 RX payload static length setting. It takes effect when DPL_P0=0.

- **RXPW1: RX Payload Length Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	RX_PW_P1[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **RX_PW_P1[5:0]**: Pipe 1 RX payload static length setting. It takes effect when DPL_P1=0.

- **RXPW2: RX Payload Length Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	RX_PW_P2[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **RX_PW_P2[5:0]**: Pipe 2 RX payload static length setting. It takes effect when DPL_P2=0.

- **RXPW3: RX Payload Length Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	—	—	RX_PW_P3[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **RX_PW_P3[5:0]**: Pipe 3 RX payload static length setting. It takes effect when DPL_P3=0.

- **RXPW4: RX Payload Length Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	—	—	RX_PW_P4[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **RX_PW_P4[5:0]**: Pipe 4 RX payload static length setting. It takes effect when DPL_P4=0.

- **RXPW5: RX Payload Length Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	—	—	RX_PW_P5[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **RX_PW_P5[5:0]**: Pipe 5 RX payload static length setting. It takes effect when DPL_P5=0.

- **ENAA: Enable Auto-ACK Control Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	ENAAP5	ENAAP4	ENAAP3	ENAAP2	ENAAP1	ENAAP0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	1	1	1

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **ENAAP[5:0]**: Auto-ACK mode enable control for Pipe 5~0
ENAAPn=0: No-Auto-ACK mode
ENAAPn=1: Enable Auto-ACK mode

- **P2B0: Pipe2 Sync Word Control Register**

Bit	7	6	5	4	3	2	1	0
Name	P2B0[7:0]							
R/W	R/W							
Reset	1	1	0	0	0	0	1	1

Bit 7~0 **P2B0[7:0]**: Receive address (sync word) LSByte in Pipe 2. MSBytes is equal to P1_SYNC[39:8].

- **P3B0: Pipe3 Sync Word Control Register**

Bit	7	6	5	4	3	2	1	0
Name	P3B0[7:0]							
R/W	R/W							
Reset	1	1	0	0	0	1	0	0

Bit 7~0 **P3B0[7:0]**: Receive address (sync word) LSByte in Pipe 3. MSBytes is equal to P1_SYNC[39:8].

- **P4B0: Pipe4 Sync Word Control Register**

Bit	7	6	5	4	3	2	1	0
Name	P4B0[7:0]							
R/W	R/W							
Reset	1	1	0	0	0	1	0	1

Bit 7~0 **P4B0[7:0]**: Receive address (sync word) LSByte in Pipe 4. MSBytes is equal to P1_SYNC[39:8].

- **P5B0: Pipe5 Sync Word Control Register**

Bit	7	6	5	4	3	2	1	0
Name	P5B0[7:0]							
R/W	R/W							
Reset	1	1	0	0	0	1	1	0

Bit 7~0 **P5B0[7:0]**: Receive address (sync word) LSByte in Pipe 5. MSBytes is equal to P1_SYNC[39:8].

- **PEN: Pipe Enable Control Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	P5ACTIVE	P4ACTIVE	P3ACTIVE	P2ACTIVE	P1ACTIVE	P0ACTIVE
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5~0 **P5ACTIVE~P0ACTIVE**: Pipe 5 ~ Pipe 0 active control
PnACTIVE=0: Pipe not active
PnACTIVE=1: Pipe active

- **XO1: XO Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	XO_IL	XO_TRIM[4:0]				
R/W	—	—	R/W	R/W				
Reset	0	0	0	1	0	0	0	0

Bit 7~6 Reserved, must be kept unchanged after power on

Bit 5 **XO_IL**: Crystal oscillator low current mode enable
0: Disable
1: Enable

Bit 4~0 **XO_TRIM[4:0]**: Trim value for the internal capacitor load for the crystal

Bank 1 Control Register

All control registers will be set to their initial value by power-on reset (POR).

Addr	Name	Bit							
		7	6	5	4	3	2	1	0
25h	RSV1	Reserved							
26h	RSV2	Reserved							
27h	RSV3	Reserved							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The recommended values for the Bank 1 registers are listed below:

Addr	Name	Setting
25h	RSV1	CCh
26h	RSV2	4Ch
27h	RSV3	80h

Bank 2 Control Register

All control registers will be set to their initial value by power-on reset (POR).

Addr	Name	Bit							
		7	6	5	4	3	2	1	0
2Dh	RSV1	Reserved							
2Eh	RSV2	Reserved							
34h	TX2	RFTXP_1							
35h	TX3	RFTXP_2							
38h	RSV3	Reserved							
39h	RSV4	Reserved							
3Bh	RSV5	Reserved							
3Ch	RSV6	Reserved							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The recommended values for the Bank 2 registers are listed below:

Addr	Name	Setting
2Dh	RSV1	18h
2Eh	RSV2	ECh
38h	RSV3	0Ah
39h	RSV4	12h
3Bh	RSV5	94h
3Ch	RSV6	43h

- **TX2: TX Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	RFTXP_1							
R/W	R/W							
Reset	1	0	1	0	1	1	1	1

- **TX3: TX Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	RFTXP_2							
R/W	R/W							
Reset	0	0	1	1	0	1	1	0

Output Power	6dBm±1	4dBm±2	0dBm±3	-5dBm±1
TX2(34h)	AF	87	63	DF
TX3(35h)	21	21	21	2F

Note: Component matching network, PCB material and layout will impact RF performance.

Functional Description

2.4GHz RF Transceiver

The BC5602 adopts a fully-integrated, low-IF receiver architecture. The received RF signal is first amplified by a low noise amplifier (LNA), after which the frequency is down-converted to an intermediate frequency (IF) by a quadrature mixer. The mixer output is filtered by a channel-selected filter which rejects the unwanted out-of-band (OOB) interference and image signals. After filtering, the IF signal is amplified by an analog programmable gain amplifier (PGA). Then the IF signal is digitized by a 9-bit ΣΔ ADC.

The BC5602 features an Automatic Gain Control (AGC) unit to adjust the receiver gain according to the RSSI, generated at the digital modem. The AGC enables the BC5602 to operate from sensitivity level to +10dBm input power.

The BC5602 adopts a fully integrated fractional-N synthesizer which includes RF VCO, loop filter and a digital controlled XO (DCXO). The fractional-N synthesizer architecture allows the users to extend their potential usage to a wider frequency range.

The transmit session is a VCO direct modulation architecture. Different from the conventional direct up-conversion transmitters, the GFSK modulation signal is fed into the VCO directly to take advantage of fractional-N synthesizer. As a result, both layout area and current consumption are much smaller compared with direct up-conversion transmitters. The fine resolution can generate a low FSK error GFSK signal. The modulated signal is fed into a Power Amplifier (PA) and the maximum output power can be up to +6dBm.

Data Control Interface – Serial Interface (SPI)

The BC5602 communicates with a host MCU via a 3-wire SPI interface (CSN, SCK, SDIO) or a 4-wire SPI interface (SDO from GIO1~GIO4) with a data rate up to 8Mbps. An SPI transmission is an (8+8×n) bits sequence which consists of an 8-bit command and n×8 bits of data, where n can be 0 or any natural number. If the number n is greater than the address boundary, the address will return to zero. The host MCU should pull the CSN (SPI chip select) pin low state in order to access the BC5602. Using the SPI interface, user can access the control registers and issue Strobe commands. When writing data to the RF chip, the SPI data will be latched into the registers at the rising edge of the SCK signal. When reading data from the RF chip registers, the bit data will be transferred at the falling edge of the SCK signal after the target register address has been input.

Command (8 Bits)								Data (8 Bits)							
C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0

SPI Command Format

Two kinds of command are defined. One is 1-byte command only, named CmdO, and the other is 1-byte command followed by n-byte data, named CmdD.

C7	C6	C5	C4	C3	C2	C1	C0	Description	CmdO	CmdD	Data Bytes
0	1	A5	A4	A3	A2	A1	A0	Write Control Register		√	1
1	1	A5	A4	A3	A2	A1	A0	Read Control Register		√	1
0	0	1	0	0	0	B1	B0	Set Register Bank	√		0
0	0	0	1	0	0	0	0	Write PRX Pipe 0 Address Write PTX Address		√	3~5
1	0	0	1	0	0	0	0	Read PRX Pipe 0 Address Read PTX Address		√	3~5
0	0	0	1	0	0	0	1	Write TX FIFO with Auto-ACK Mode Command		√	1~32
1	0	1	1	1	1	1	1	Read RX FIFO Command		√	1~32
0	0	0	1	0	0	1	0	Write PRX Pipe 1 Address		√	3~5
1	0	0	1	0	0	1	0	Read PRX Pipe 1 Address		√	3~5
0	0	0	1	0	0	1	1	Write TX FIFO with No-Auto-ACK Mode Command		√	1~32
0	0	0	1	1	0	0	0	Write Pipe 0 ACK Payload Command		√	1~32
0	0	0	1	1	0	0	1	Write Pipe 1 ACK Payload Command		√	1~32
0	0	0	1	1	0	1	0	Write Pipe 2 ACK Payload Command		√	1~32
0	0	0	1	1	0	1	1	Write Pipe 3 ACK Payload Command		√	1~32
0	0	0	1	1	1	0	0	Write Pipe 4 ACK Payload Command		√	1~32
0	0	0	1	1	1	0	1	Write Pipe 5 ACK Payload Command		√	1~32
0	0	0	0	1	0	0	0	Software Reset Command	√		0
0	0	0	0	1	0	0	1	TX FIFO Flush Command	√		0
1	0	0	0	1	0	0	1	RX FIFO Flush Command	√		0
0	0	0	0	1	0	1	0	Deep Sleep Mode Setting Command	√		0
0	0	0	0	1	1	0	0	Light Sleep Mode Setting Command	√		0
0	0	0	0	1	1	0	1	Standby Mode Setting Command	√		0
0	0	0	0	1	1	1	1	Middle Sleep Mode Setting Command	√		0
0	0	0	0	1	1	1	0	TX Mode Trigger Command	√		0
1	0	0	0	1	1	1	0	RX Mode Trigger Command	√		
1	0	0	1	1	1	1	1	Read Chip Version		√	3

Strobe Commands Table

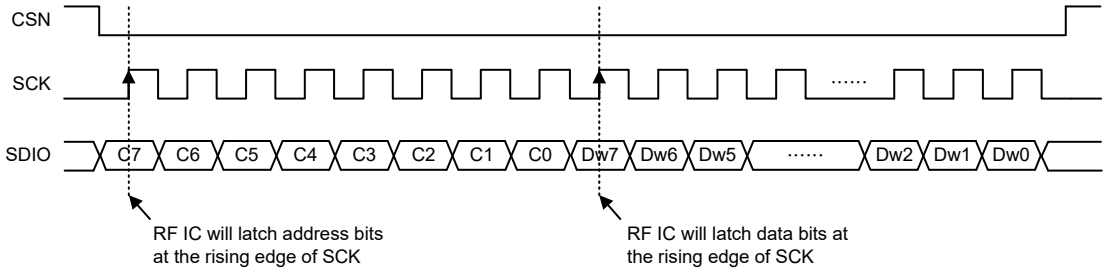
A5~A0: The address of control register

B1~B0: Bank number

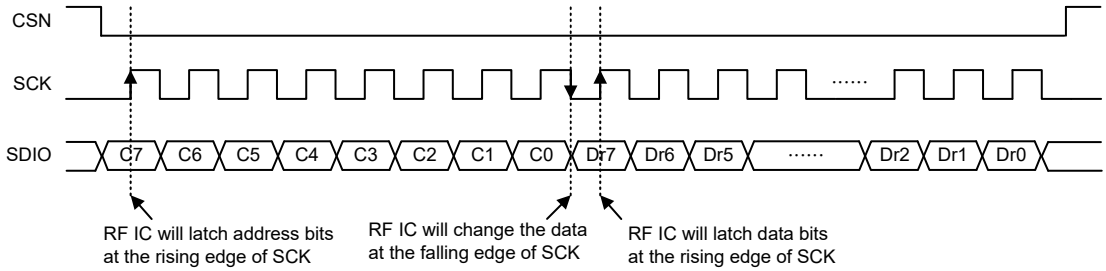
Note: 1. The chip supports multi-byte read/write operations and the address is increased automatically after each read or write operation.

2. Using software to read/write multiple bytes is allowed after one read/write command in a single CSN enabled cycle.

SPI Timing

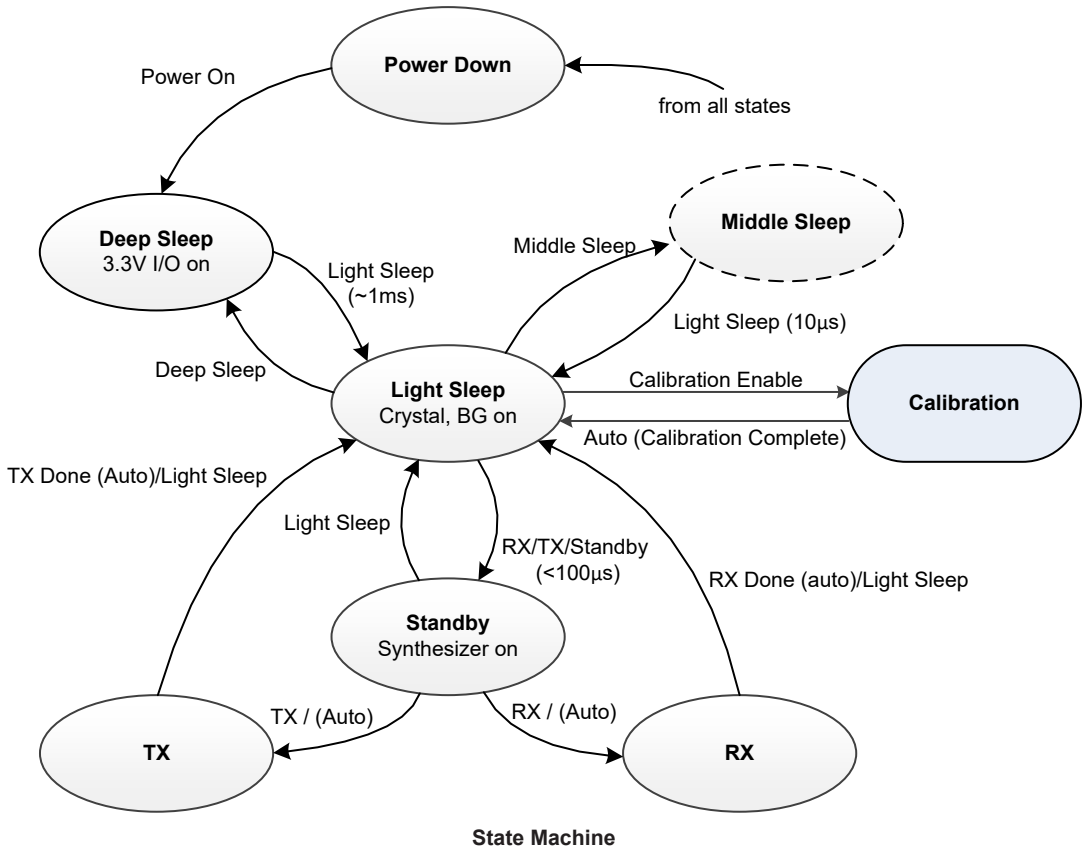


3-Wire SPI Interface Write 1-byte Data Operation



3-Wire SPI Interface Read 1-byte Data Operation

State Machine



State Machine

There are eight operating modes in the BC5602 from the viewpoint of current consumption, as listed below.

1. Power Down state
2. Deep Sleep state: 3.3V I/O on
3. Light Sleep state: BG (Bandgap) and XO on
4. Standby state: Synthesizer on
5. Calibration state
6. Middle Sleep state: Lower current consumption than light Sleep state function is on
7. TX state
8. RX state

State	Register Retention	3.3V	Lower XTAL Drive	Regulator	XTAL	Standby + VCO	TX	RX	Strobe Command
Power Down	No	Off	Off	Off	Off	Off	Off	Off	—
Deep Sleep	Yes	On	Off	Off	Off	Off	Off	Off	8'b0000_1010
Light Sleep	Yes	On	Off	On	On	Off	Off	Off	8'b0000_1100
Middle Sleep	Yes	On	On	Off	Off	Off	Off	Off	8'b0000_1011
Standby	Yes	On	Off	On	On	On	Off	Off	8'b0000_1101
TX	Yes	On	Off	On	On	On	On	Off	8'b0000_1110
RX	Yes	On	Off	On	On	On	Off	On	8'b1000_1110

Power Down State

In the Power Down state, the device is disabled without power supply.

Deep Sleep State

After power on, the device completes the internal power on reset then the system will stay in the Deep Sleep mode to wait further SPI commands from the host MCU and keep a minimum current consumption, the SPI remain active as well. When the SPI CSN pin is detected changing from high to low, the system will enable the internal LDO, bring up XTAL and stay in the Light Sleep state.

Light Sleep State

In the Light Sleep state, both of XTAL and BG are on and ready for TX/RX operation. In this state, the host MCU can have the BC5602 do calibration process if necessary. By issuing the Deep Sleep setting command, the device will power down the LDO and XO and enter the Deep Sleep state. After the TX/RX completion, the device will return to the Light Sleep mode.

Middle Sleep State

For further current consumption reduction of the Light Sleep mode, the device supports low current Middle Sleep mode. In this state, the system will keep XTAL on in order to be woken up immediately but with lower XTAL driving for power saving by issuing the Middle Sleep mode setting command. The current is less than 30μA in the Middle Sleep mode and the chip could quickly return (<10μs) to the Light Sleep state after receiving the Light Sleep setting command. In the Middle Sleep mode, the whole system is idle with only XTAL running under the bleeding current.

Calibration State

There is a VCO calibration function built in the chip to assist users to auto select proper setting to compensate the PVT (Process-Voltage-Temperature) variation effect. The host MCU can enable the calibration by setting the ACAL_EN bit and poll the ACAL_EN bit status until ACAL_EN is reset by hardware indicating that the calibration is complete.

The calibration function can only be activated in the Light Sleep state.

To get an accurate RF frequency, an appropriate VCO curve needs to be set by the VCO calibration process. After power on, the host MCU needs to do VCO calibration after setting the RF synthesizer frequency. To initiate VCO calibration, the host MCU needs to follow the procedure as shown below.

1. To select the RF channel (RF_CH): RF Carrier = 2400MHz + RF_CH (RF_CH = 0~100, channel step: 1MHz)
2. Set ACAL_EN=1 to start VCO calibration.
3. Polling the ACAL_EN until it is cleared to 0 to detect the VCO calibration completion.

Standby State

After the host triggers the BC5602 TR/RX operations in the Light Sleep state, the BC5602 starts the synthesizer and enters the standby state when the synthesizer is stable. Then the BC5602 starts normal TR/RX operations.

TX State

The device will enter the TX state in the following conditions.

1. Continuous mode: PRM_RX is set to 0, CE is set to 1 and TX FIFO is not empty.
2. Single strobe mode: PRM_RX is set to 0 and a TX command is received.

The device will stay in the TX state for transmission until a complete TX packet is transmitted, then it returns to the Light Sleep state. If CE=1 and TX FIFO is still not empty, the device will automatically trigger next TX transaction.

The modulator and radio PA are active in the TX state.

RX State

The device will enter the RX state in the following conditions which are all in the continuous mode.

1. PRM_RX is set to 1 and CE is set to 1.
2. PRM_RX is set to 1 and a RX command is received. On receiving the RX command, CE will be set to 1 automatically.

The system will stay in the RX state until an RX complete event happens, then the device returns to the Light Sleep state. An RX complete event can be that an RX packet is successfully received or an RX time out condition happens.

The demodulator, Radio LNA and Mixer are active in the RX state.

RF Channel Frequency and Data Rate

RF Channel Frequency

The BC5602 RF channel frequency is determined by the carrier frequency, the modulated RF signal occupies a BW which is less than 1MHz at 125/250/500Kbps data rate. It operates in a frequency ranges from 2400MHz to 2500MHz. The programmable resolution of RF channel frequency is 1MHz. The RF_CH register defines the RF channel as the following formula:

$$fc = 2400 + RF\_CH\ (MHz)$$

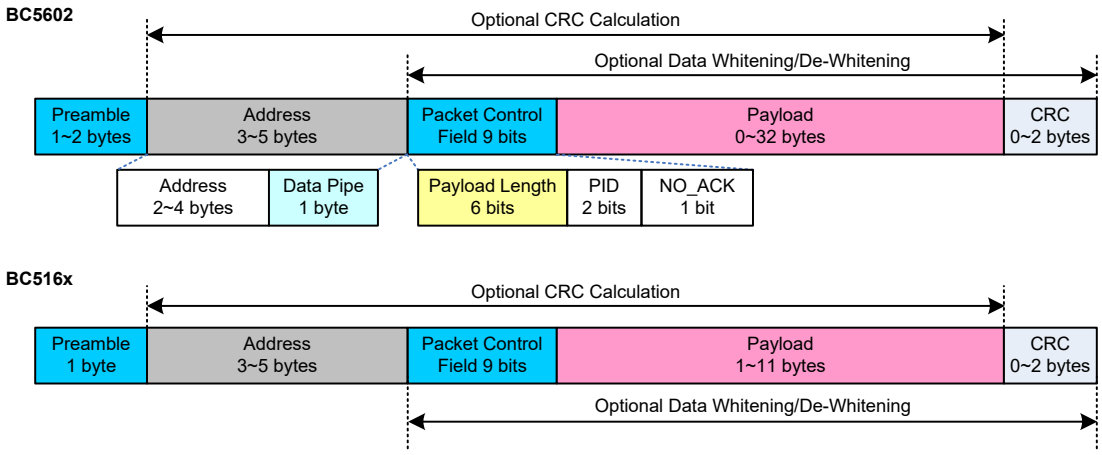
In order to communicate with each other, the RF_CH of both sides of the transceiver should be set with the same value.

RF Data Rate

The Data Rate of the device is programmable, which is 125/250/500Kbps.

Packet Format

The BC5602 supports Burst mode packet format as shown in the figure below. The 9-bit Packet Control Field (PCF) is optional and is enabled by default to be compatible with the BC516x series. So the BC5602 can act the role of receiver to pair with the BC516x without responding the ACK packet to the BC516x by following the hopping type protocol of the BC516x.



Bit Ordering

The bit ordering transmitted over the air follows the rule as shown below.

1. Preamble is transmitted the most significant first.
2. Address is transmitted starting from the most significant byte with the most significant bit first.
3. Packet Control Field is transmitted with the most significant bit first.
4. Payload is transmitted starting from the least significant byte with the most significant bit first.
5. CRC field is transmitted starting from the most significant byte with the most significant bit first.

Preamble Field

The BC5602 has 1~2 bytes of Preamble. The bit sequence is either 01010101(LSB) or 10101010(LSB) for the 1-byte Preamble. For the 2-byte Preamble, the bit sequence is either 01010101_01010101(LSB) or 10101010_10101010(LSB). Users can set Preamble Length to one or two bytes by setting the AMBLE2 bit. This sequence is determined by the first transmitted bit of the Address. The definition is listed below.

1st transmitted bit of Address:

0: Preamble = 01010101(LSB) /
01010101_01010101(LSB)

1: Preamble = 10101010(LSB) /
10101010_10101010(LSB)

Address Field

An address ensures that the packet is detected by the target receiver. The address field can be configured to be 3, 4, or 5 bytes long using the AW[1:0] bit field.

The PRX device can open up to six data pipes to support up to six PTX devices each with a unique address. All six PTX device addresses are searched simultaneously. For the PRX side, the data pipes are enabled using the bits in the PEN register. By default, only data pipe 0 and 1 are enabled. Each pipe can have up to 5 bytes of configurable address. Pipe 0 and 1 have their corresponding commands to configure the address. Data pipe 0 has a fully unique address. Data pipes 1~5 share the common four most significant address bytes. The least significant byte must be unique for pipes 1~5. The least significant address byte of pipe 2~5 is configured in the PnB0 (n=2~5) register respectively. To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet.

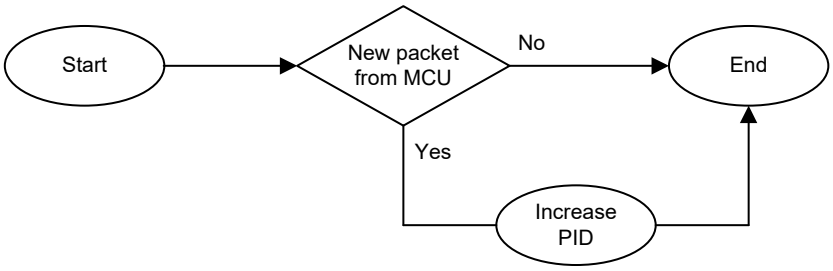
Packet Control Field – PCF

The Packet Control Field is a 9-bit long field which defines “Payload length”, “PID” and “NO_ACK”, the description are as follows:

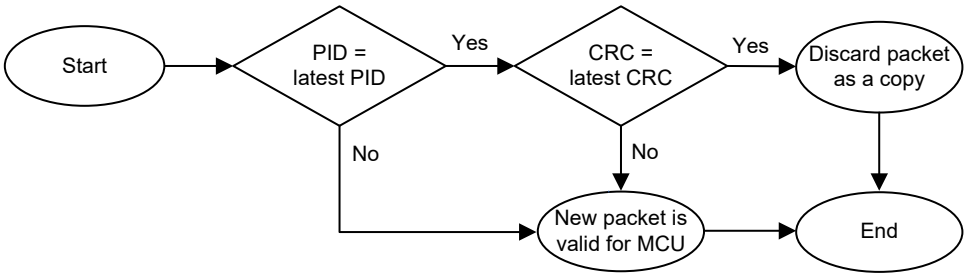
- Payload Length: 6 bits
  The Payload length is calculated automatically by the BC5602 depending on the packet format of the IC. The payload length can be 0 to 32 bytes. Length 0 is only valid for the ACK packet without payload. The packet from PTX to PRX has a valid payload of 1 to 32 bytes.
- PID (Packet Identification): 2 bits
  This PID is a 2-bit long Packet Identification filed which is used to help the receiver to distinguish if a new packet or a repeated packet is received. The PTX increases the PID when sending a new packet from the MCU.

  Working together with the auto-acknowledge and auto-retransmission features, the PID of the BC5602 starts with 0 and increases by 1 for the next new packet if a ACK packet is received. If the packet has been sent but the ACK packet has not been received for a period of time (ARD[3:0]), according to the Auto Resend times defined by ARC[3:0], the system will retransmit the packet with the same PID of the last packet until a ACK packet from the receiver is received or until the resending times are finished. In order to keep the PID sequence correct, the PID will not be reset in the Deep Sleep mode.

PTX Functionality



PRX Functionality



- NO_ACK: 1 bit

  This field is a 1-bit no acknowledge indication flag. The NO_ACK flag is only used when the auto-acknowledgement feature is enabled. Setting the flag high will inform the receiver that the packet is not to be auto-acknowledged.

  The PTX can set the NO_ACK bit in the Packet Control Field using the W_TX_PAYLD_NO_ACK command. However, this command function must first be enabled by setting the EN_DYN_ACK bit in the DPL2 register. When no acknowledge option is used, the PTX directly enters the Light Sleep state after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet. There is an extra INV_NOACK control bit to set the active polarity of the NO_ACK flag. If the INV_NOACK bit is set to 1, the NO_ACK flag could not be set high by W_TX_PAYLD_NO_ACK to indicate no acknowledge requirement.

	DPL2: INV_NOACK=0	DPL2: INV_NOACK=1
PTX: W_TX_PAYLD_NO_ACK	TX with NO_ACK=1	TX with NO_ACK=0
PTX: W_TX_PAYLD	TX with NO_ACK=0	TX with NO_ACK=1
PRX's ENAA is set	ACK when receiving NO_ACK=0	ACK when receiving NO_ACK=1

Payload Field

The payload is the user-defined content of the packet. It can be 0 to 32 bytes wide, and it is transmitted on-air as it is uploaded (unchangable) to the device.

The BC5602 provides two alternatives for handling payload lengths, static and dynamic payload length. The static payload length of each of six data pipes can be individually set. The default option is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Pn (n=0~5) register. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must be equal to the value in the RX_PW_Pn register on the receiver side. Each pipe has its own payload length.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with a variable payload length to the receiver.

With DPL feature the BC5602 can decode the payload length of the received packet automatically instead of using the RX_PW_Pn registers. The MCU can read the length of the received payload by reading the RXDLEN field.

In order to enable DPL, the EN_DPL bit in the DPL2 register must be set high. In RX mode the DPL_Pn (n=0~5) bits in the DPL1 register has to be set high. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DPL1 set. The DPL mode not supported in ENAA=0.

CRC Field

The CRC is the error detection mechanism in the packet. The number of bytes in the CRC is set by the CRC control bits in the PKT1 register. It may be either 1 or 2 bytes and is calculated over the address, Packet Control Field and Payload.

The polynomial and initial value for 1 byte and 2 bytes of CRC and CRC function disabled are list as shown in the table below.

No packet is accepted by the receiver side if the CRC is enabled and fails (either 1 byte or 2 bytes).

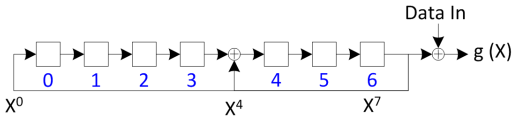
CRC	Polynomial	CRC Control Bits		Description / Formula	Initial Value
		CRC8_EN	CRC_EN		
Disable	/	X	0	CRC is disabled	X
CRC-8	0x07	1	1	$X^8 + X^2 + X + 1$	FFh
CRC-CCITT	0x1021	0	1	$X^{16} + X^{12} + X^5 + 1$	FFFFh

X: don't care

Security Function

The security function, which is optional and is set by the WHT_EN bit, is implemented by LFSR (Data Whitening/De-Whitening) for the BC5602. The formula listed below calculates both of payload and CRC field (Data In). The Packet Encryption Key is WHT_PTN[6:0], its initial value is WHTSD[6:0].

$g(X) = X^7 + X^4 + 1$



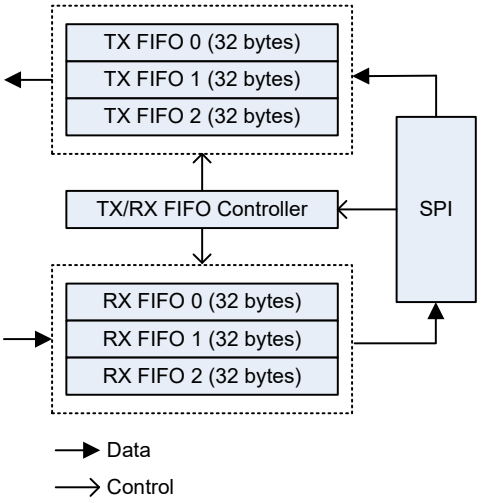
X^0: WHT_PTN[0]
X^1: WHT_PTN[1]
X^2: WHT_PTN[2]
X^3: WHT_PTN[3]
X^4: WHT_PTN[4]
X^5: WHT_PTN[5]
X^6: WHT_PTN[6]

Data FIFO

TX/RX FIFO

The BC5602 contains three levels of 32-byte data FIFO for transmitting payload of TX and receiving payload of RX.

- TX three levels, 32-byte FIFO
- RX three levels, 32-byte FIFO



Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands.

The FIFOs are accessible in both PTX and PRX mode. TX FIFO and RX FIFO each have three levels and each FIFO level size is 32 bytes at most.

Users can use three commands to write TX payloads into TX FIFO, which are Write TX FIFO with Auto-ACK Mode Command and Write TX FIFO with No-Auto-ACK Mode Command for the PTX device, and Write Pipe N ACK Payload Command for the PRX device. If the TX FIFO in a PTX device contains more than one payload to a pipe, the payloads will be handled in a "first in - first out" mode. The TX FIFO in a PRX device will be used to acknowledge the corresponding pipe.

The RX FIFO in a PRX device can contain the received payloads from up to three different PTX devices. If RX FIFOs are full, the new receiving data on-air will be lost. Users can use "Read RX FIFO Command" to read RX payloads in both PTX and PRX devices. The STATUS register shows the FIFO's status.

FIFO Flush

If link layer failed or other reasons cause FIFO data useless, users can use "TX FIFO Flush Command" to reset the TX FIFO, or use the "RX FIFO Flush Command" to reset the RX FIFO. After using the flush command, the FIFO's status will be empty.

Interrupt

The BC5602 has an Interrupt Request (IRQ) pin which is low active and is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ in the IRQ1 register is set high by the state machine. The IRQ pin is reset when the MCU writes '1' to the IRQ source bit in the IRQ1 register. The IRQ mask in the MASK register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the mask bits high, the corresponding IRQ source is disabled. All IRQ sources are enabled by default.

The 3-bit pipe information in the IRQ1 register is updated during the IRQ pin high to low transition. If the IRQ1 register is read during an IRQ pin high to low transition, the pipe information is unreliable.

One-to-Six Star Network

The BC5602 can be configured as PRX that can receives data from up to 6 different data pipes at one frequency. Each pipe has its own data pipe address. The address length can be configured as 3~5 bytes long and all data pipes adopt the same address length configuration. Up to 6 PTX devices with different addresses can communicate with a PRX.

For the PRX side, the data pipes are enabled with the bits in the PEN register. Only data pipe 0 and 1 are enabled by default.

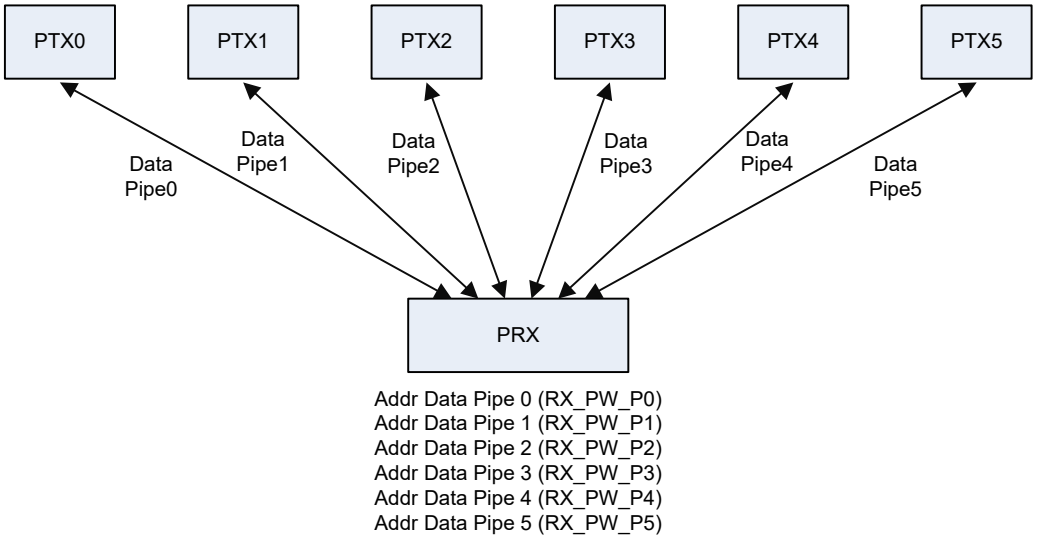
Pipe 0 address is written by the Write PRX Pipe 0 Address Command. Pipe 1 address is written by the Write PRX Pipe1 Address Command. The data pipe 0 has a unique full address setting. The most significant 16 bits of the address cannot be the same for pipe 0 and pipe 1. The LSByte of pipe 2~5 addresses are set by writing the PnB0 (n=2~5) control registers. The data pipes 1~5 share the same most four significant address bytes and are distinguished by a different least significant address byte.

The following table lists a PRX pipe address setting example.

	Byte4	Byte3	Byte2	Byte1	Byte0
Data pipe 0 (Strobe Command Pipe 0)	0xF1	0xD2	0xE6	0xA2	0x33
Data pipe 1 (Strobe Command Pipe 1)	0x7F	0xFE	0x8E	0x47	0xD3
Data pipe 2 (P2B0)	↑	↑	↑	↑	0xD4
Data pipe 3 (P3B0)	↑	↑	↑	↑	0xD5
Data pipe 4 (P4B0)	↑	↑	↑	↑	0xD6
Data pipe 5 (P5B0)	↑	↑	↑	↑	0xD7

The data pipes are enabled, data pipe 0 has a 5-byte address and pipes 1 to 5 share the four most significant address bytes, i.e., the address byte 1 to 4 are the same but the byte 0 of all six pipes' addresses must be different.

When PRX receives a valid payload, it will record the corresponding PTX's address. Then PRX uses the recorded address to acknowledge PTX if the auto-acknowledgement feature is enabled. When PTX uses pipe 0 for receiving acknowledge packet, the PTX needs to use the same address for pipe 0 and TX packet. The following diagram shows a setting example for PTX and PRX.



Abbreviation

ACK: Acknowledgement

ADC: Analog to Digital Converter

AFC: Automatic Frequency Compensation

AGC: Automatic Gain Control

ARC: Auto Resend Count

ARD: Auto Resend Delay

BER: Bit Error Rate

BG: Gandgap

BPF: Band Pass Filter

BW: Bandwidth

CD: Carrier Detect

CFO: Carrier Frequency Offset

CP: Charge Pump

CRC: Cyclic Redundancy Check

DCOC: DC Offset Correct

DSM: Delta Sigma Modulator

FEC: Forward Error Correction

GFSK: Gaussian Frequency Shift Keying

IF: Intermedia Frequency

IRQ: Interrupt Request

ISM: Industrial, Scientific and Medical

LFSR: Linear Feedback Shift Register

LNA: Low Noise Amplifier

LO: Local Oscillator

MCU: Micro Controller Unit

MMD: Multi-Mode Divider

PA: Power Amplifier

PCF: Packet Control Field

PD: Power Down

PFD: Phase Frequency Detector

PID: Packet Identity Bits

PLD: Payload

PLL: Phase Lock Loop

POR: Power On Reset

PRX: Primary RX

PTX: Primary TX

PVT: Process-Voltage-Temperature

RF_CH: Radio Frequency Channel

RSSI: Received Signal Strength Indicator

RX: Receiver

SX: Synthesizer

SYCK: System Clock for digital circuit

TRX: TX/RX

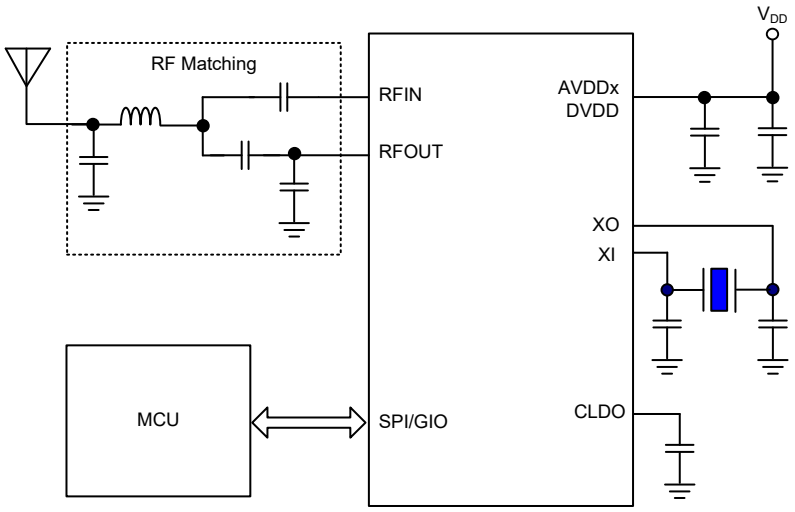
TX: Transmitter

VCO: Voltage Controlled Oscillator

XCLK: Crystal Clock

XO/XTAL: Crystal Oscillator

Application Circuit



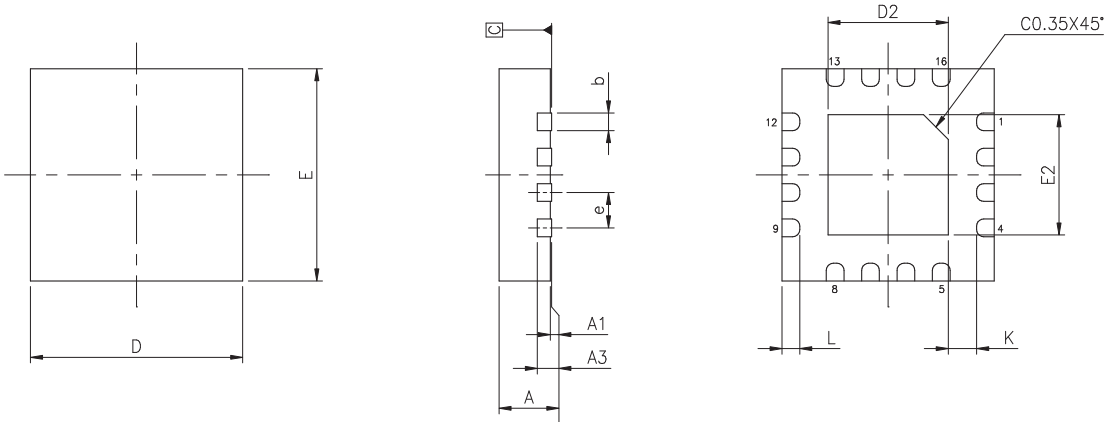
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

SAW Type 16-pin QFN (3mm×3mm for FP0.25mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.007	0.010	0.012
D	—	0.118 BSC	—
E	—	0.118 BSC	—
e	—	0.020 BSC	—
D2	0.063	0.067	0.069
E2	0.063	0.067	0.069
L	0.008	0.010	0.012
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.200 BSC	—
b	0.180	0.250	0.300
D	—	3.000 BSC	—
E	—	3.000 BSC	—
e	—	0.50 BSC	—
D2	1.60	1.70	1.75
E2	1.60	1.70	1.75
L	0.20	0.25	0.30
K	0.20	—	—